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CV

Standard DRAC form

Number of pages: 33

First name and surnames: Francesc de Borja Moll Echeto

Date: 20 November 2024

Signature: Moll, F.

The undersigned hereby states that the information in this CV is true and is notified that she/he shall be held liable for any claims arising from inaccuracies and that she/he may be subject to requests for further information or proof of veracity during the assessment process.

You must sign in the margin of every page.

1. Personal details

Surnames and first name		ID / Passport number
Moll Echeto Francesc de Borja		
Nationality	**Date of birth**	**Sex**
Espanya		
Address		

2. Current job status

Institution / Organization / company Universitat Politècnica de Catalunya	**School** Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona (ETSETB)
Department / section / unit Departament d'Enginyeria Electrònica	
Post held Associate professor	**Start date** 01-02-1997
Administrative status Publicly contracted	
Commitment Full-time	**Specialization (UNESCO codes)** 330793 Microelectronics: Design; 330700 Electronic technology (see 2202, 2203, 3311.07, 3325); 220307 Integrated circuits (see 3307.03)
Institution / Organization / company Barcelona Supercomputing Center-Centro Nacional de Supercomputación	**School**
Department / section / unit	
Post held Associate professor	**Start date** 01-07-2022
Administrative status Publicly contracted	
Commitment Full-time	**Specialization (UNESCO codes)** 330793 Microelectronics: Design; 330700 Electronic technology (see 2202, 2203, 3311.07, 3325); 220307 Integrated circuits (see 3307.03)
Institution / Organization / company Universitat Politècnica de Catalunya	**Department / section / unit** Departament d'Enginyeria Electrònica
Post held Sotsdirector/a Del Departament	**Start date** 09-04-2018
Administrative status Others	**Commitment** Full-time
Institution / Organization / company Universitat Politècnica de Catalunya	**Department / section / unit** Departament d'Enginyeria Electrònica
Post held Sotsdirector/a de Departament	**Start date** 09-04-2018
Administrative status Others	**Commitment** Full-time

3. Education

Undergraduate degree / 1st cycle / 1st and 2nd cycle / 2nd cycle	School	Date of graduation
CIENCIES FISIQUES	UIB	30-06-1990

Doctoral degree	School	Date of graduation
CIENCIES FISIQUES	Universitat Politècnica de Catalunya	31-03-1995

Other postgraduate qualifications	School	Date of graduation

4. Scientific or professional activities prior to current status

Category	Institution	Period
		-
		-

5. Languages

Language	Listening comprehension	Reading comprehension	Written expression	Oral expression	Oral interaction
English	B1	C1	C1	C1	C1

A. Publications

A.1 Journal papers

Arnaiz, D.; Moll, F.; Alarcon, E.; Vilajosana, X. **Energy and relevance-aware adaptive monitoring method for wireless sensor nodes with hard energy constraints.** *Integration (Amsterdam)*. 2024. Volume: 94. Number: article 102097. <https://doi.org/10.1016/j.vlsi.2023.102097>

Fornt, J.; Fontova, P.; Caro, M.; Abella, J.; Moll, F.; Altet, J.; Studer, C. **An energy-efficient GeMM-based convolution accelerator with on-the-fly im2col.** *IEEE transactions on very large scale integration (VLSI) systems*. 2023. Volume: 31. Number: 11. pp.: 1874 ~ 1878. <https://doi.org/10.1109/TVLSI.2023.3286122>

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Minervini, F.; Palomar, Ó.; Unsal, O.; Reggiani, E.; Quiroga, J.; Marimon, J.; Rojas, C.; Figueras, R.; Ruíz, A.; González, A.; Mendoza, J.; Vargas, I.; Hernández, C.; Cabré, J.; Khoirunisya, L.; Bouhali, M.; Pavón, J.; Moll, F.; Olivieri, M.; Kovac, M.; Kovac, M.; Dragic, L.; Valero, M.; Cristal, A. **Vitruvius+: An area-efficient RISC-V decoupled vector coprocessor for high performance computing applications.** *ACM transactions on architecture and code optimization*. 2023. Volume: 20. Number: 2, article 28. pp.: 1 ~ 25. <https://doi.org/10.1145/3575861>

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López, P.; Gabilondo, I.; Alarcon, E.; Moll, F. **Mechanical energy harvesting taxonomy for industrial environments: application to the railway industry.** *IEEE transactions on intelligent transportation systems*. 2020. Volume: 21. Number: 7. pp.: 2696 ~ 2706. <https://doi.org/10.1109/TITS.2019.2924987>

Calomarde, A.; Rubio, A.; Moll, F.; Gamiz, F. **Active radiation-hardening strategy in bulk FinFETs.** *IEEE access*. 2020. Volume: 8. pp.: 201441 ~ 201449. <https://doi.org/10.1109/ACCESS.2020.3035974>

Escudero, M.; Vourkas, I.; Rubio, A.; Moll, F. **Memristive logic in crossbar memory arrays: Variability-aware design for higher reliability.** *IEEE transactions on nanotechnology*. 2019. Volume: 18. pp.: 635 ~ 646. <https://doi.org/10.1109/TNANO.2019.2923731>

Nunes, D.; Moll, F.; Valtchev, S. **Prospects of Tunnel FETs in the design of power management circuits for**

weak energy harvesting dc sources. *IEEE Journal of the Electron Devices Society*. 2018. Volume: 6. Number: 1. pp.: 382 ~ 391. <https://doi.org/10.1109/JEDS.2018.2808950>

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Calomarde, A.; Amat, Esteve; Moll, F.; Vigara, J.; Rubio, A. **SET and noise fault tolerant circuit design techniques: application to 7 nm FinFET.** *Microelectronics reliability*. 2014. Volume: 54. Number: 4. pp.: 738 ~ 745. <https://doi.org/10.1016/j.microrel.2013.12.018>

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Amat, Esteve; Amatlle, E.; Gómez, S.; Aymerich, N.; Garcia, C.; Moll, F.; Rubio, A. **Systematic and random variability analysis of two different 6T-SRAM layout topologies.** *Microelectronics journal*. 2013. Volume: 44. Number: 9. pp.: 787 ~ 793. <https://doi.org/10.1016/j.mejo.2013.06.010>

Gomez, S.; Moll, F. **Yield estimation model for lithography hotspot distortions.** *Electronics letters*. 2013. Volume: 49. Number: 17. pp.: 1066 ~ 1068. <https://doi.org/10.1049/el.2013.0469>

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Auguet, C.; Martorell, F.; Moll, F.; Torra, V. **Identification of micro-scale calorimetric devices II. Heat transfer models from two- or three- dimensional analysis.** *Journal of thermal analysis and calorimetry*. 2002. Volume: 70. Number: 1. pp.: 277 ~ 290. <https://doi.org/10.1023/A:1020642709172>

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Moll, F.; Roca Vallmajor, Antoni; Rubio, A. **Measurement of crosstalk-induced delay errors in integrated circuits.** *Electronics letters*. 1997. Volume: 33. Number: 19. pp.: 1623 ~ 1624.

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A.2 Conference papers

Pavón, J.; Vargas, I.; Rojas, C.; Hernández, C.; Aslan, M.; Figueras, R.; Yuan, Y.; Lindegger, J.; Alser, M.; Moll, F.; Marco, S.; Ergin, O.; Talati, N.; Mutlu, O.; Unsal, O.; Valero, M.; Cristal, A. **QUETZAL: Vector acceleration framework for modern genome sequence analysis algorithms**. *2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture, ISCA 2024: 29 June–3 July 2024, Buenos Aires, Argentina: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2024. pp.: 597 ~ 612. ISBN/ISSN: 979-8-3503-2658-1. <https://ieeexplore.ieee.org/xpl/conhome/10609566/proceeding>

Doblas, M.; Candón, G.; Carril Gil, X.; Domínguez, M.; Erra, E.; González, A.; Jiménez, V.; Kostalampros, I.; Langarita, R.; Leyva, N.; López-Paradís, G.; Mendoza, J.; Oltra-Oltra, J.; Pavón, J.; Ramírez, C.; Rodas, N.; Reggiani, E.; Rodriguez, M.; Rojas, C.; Ruiz, A.; Safadi, H.; Soria, V.; Vargas, I.; Arreza, F.; Figueras, R.; Fontova, P.; Marimon, J.; Aragones, X.; Cristal, A.; Mateo, D.; Moll, F.; Moreto, M.; Palomar, Ó.; Sonmez, Nehir; Unsal, O.; Valero, M. **Sargantana: an academic SoC RISC-V processor in 22nm FDSOI technology**. *38th Conference on Design of Circuits and Integrated Systems (DCIS 2023): Pamplona, Spain: November 15-17, 2023: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2023. ISBN/ISSN: 979-8-3503-0385-8. <https://ieeexplore.ieee.org/xpl/conhome/10335898/proceeding>

Arnaiz, D.; Vila, M.; Alarcon, E.; Moll, F.; Sancho, Maria-Ribera; Teniente, E. **Relating context and self awareness in the Internet of Things**. *Cooperative Information Systems: 29th International Conference, CoopIS 2023: Groningen, The Netherlands: october 30-november 3, 2023: proceedings*. Springer. 2023. pp.: 384 ~ 402. ISBN/ISSN: 978-3-031-46846-9. <https://link.springer.com/book/10.1007/978-3-031-46846-9>

Fornt, J.; Fontova, P.; Caro, M.; Abella, J.; Moll, F.; Altet, J.; Rubio, A. **Energy efficient object detection for automotive applications with YOLOv3 and approximate hardware**. *2023 IEEE 23rd International Conference on Nanotechnology (IEEE-NANO 2023): Jeju, Korea: July 2-5, 2023: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2023. pp.: 592 ~ 595. ISBN/ISSN: 979-8-3503-3347-3. <https://doi.org/10.1109/NANO58406.2023>

Pavón, J.; Vargas, I.; Marimon, J.; Figueras, R.; Moll, F.; Unsal, O.; Valero, M.; Cristal, A. **VAQUERO: A scratchpad-based vector accelerator for query processing**. *2023 IEEE International Symposium on High-Performance Computer Architecture (HPCA): Montreal, QC, Canada, 25 February-1 March 2023: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2023. pp.: 1289 ~ 1302. ISBN/ISSN: 978-1-6654-7652-2. <https://ieeexplore.ieee.org/xpl/conhome/10070856/proceeding>

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Fornt, J.; Jin, L.; Etxezarreta, I.; Fontova, P.; Altet, J.; Calomarde, A.; Morancho, E.; Moll, F.; Rubio, A. **Two examples of approximate arithmetic to reduce hardware complexity and power consumption**. *DCIS 2022: proceedings of the 37th Conference on Design of Circuits and Integrated Systems: Pamplona, Navarra, 16-18 November 2022*. Institute of Electrical and Electronics Engineers (IEEE). 2022. pp.: 1 ~ 6. ISBN/ISSN: 978-1-6654-5950-1. <https://ieeexplore.ieee.org/xpl/conhome/9969904/proceeding>

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Pavón, J.; Vargas, I.; Barredo, A.; Marimon, J.; Moreto, M.; Moll, F.; Unsal, O.; Valero, M.; Cristal, A. **VIA: A smart scratchpad for vector units with application to sparse matrix computations**. *27th IEEE International Symposium on High Performance Computer Architecture: 27 February-3 March 2021, virtual event: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2021. pp.: 921 ~ 934. ISBN/ISSN: 978-0-7381-2337-0. <https://ieeexplore.ieee.org/xpl/conhome/9406784/proceeding>

Arnaiz, D.; Moll, F.; Alarcon, E.; Vilajosana, I. **Data relevance-aware dynamic sensing technique with battery lifetime guarantee for wireless sensor nodes**. *XXXVI Conference on Design of Circuits and Integrated Systems (DCIS 2021): Vila do Conde, Portugal: november 24-26, 2021: proceedings*. Institute of Electrical and Electronics Engineers (IEEE). 2021. pp.: 1 ~ 6. ISBN/ISSN: 978-1-6654-2116-4. <https://doi.org/10.1109/DCIS53048.2021>

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Barajas, E.; Aragones, X.; Mateo, D.; Moll, F.; Rubio, A.; Martin, J.; Rodríguez, R.; Porti, M.; Nafria, M.; Castro Lopez, R.; Roca, E.; Fernandez, F. **Analysis of body bias and RTN-induced frequency shift of low voltage ring oscillators in FDSOI technology**. *2018 IEEE 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS 2018): 2-4 July 2018, Spain*. Institute of Electrical and Electronics

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Marin-Martinez, J.; Rodriguez, R.; Nafría, M.; Torrents, G.; Bota, S.A.; Segura, J.; Moll, F.; Rubio, A. **Statistical characterization and modeling of random telegraph noise effects in 65nm SRAM cells**. *SMACD 2017: 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design: 12th-15th June 2017: Giardini Naxos, Taormina, Itlaly*. Institute of Electrical and Electronics Engineers (IEEE). 2017. pp.: 1 ~ 4. ISBN/ISSN: 978-1-5090-5052-9. <http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7970054>

Rubio, A.; Moll, F.; Escudero, M.; Zuin, S.; Vourkas, I.; Sirakoulis, G. **Experience on material implication computing with an electromechanical memristor emulator**. *Proceedings SSCI 2016*. Institute of Electrical and Electronics Engineers (IEEE). 2016. pp.: 170 ~ 175. ISBN/ISSN: 978-1-5090-4240-1. <http://ieeexplore.ieee.org/Xplore/home.jsp>

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A.3 Conference proceedings (editor)

A.4 Books

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A.5 Book chapters

Fornt, J.; Jin, L.; Altet, J.; Moll, F.; Rubio, A. **Evaluation of the functional impact of approximate arithmetic circuits on two application examples.** *Design and applications of emerging computer systems*. Springer. 2024. pp.: 421 ~ 451. ISBN: 978-3-031-42477-9. <https://doi.org/10.1007/978-3-031-42478-6>

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A.6 Publication of exhibition catalogue

A.7 Authorship of exhibition catalogue chapters

A.8 Other scientific and technical documents

Palma, K.; Moll, F. **Semi-analytic discrete time model of a 1-stage CC-CP.** 20/11/2019. pp.: 4. <http://hdl.handle.net/2117/366462>

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A.9 Theses

Moll, F. **Parasitic Effects Due to Interconnections in Microelectronic Design. Doctoral thesis**. 31/03/1995. Mark: Excellent Cum Laude. Supervisor/s: Rubio, A.. Universitat Politècnica de Catalunya.

A.10 Teaching materials or lecture notes

Rubio, A.; Altet, J.; Aragones, X.; Gonzalez, J.; Diego, M.; Moll, F. **Practiques de Laboratori de l'assignatura DCiSE.** Laboratory practicals. 2003.

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A.11 Other written output / Preprints

B. Conferences, courses and other events

B.1 Presentation of conference papers

Moll, F. **Experimental Runtime Power Measurements in Wireless Sensor Networks**. *I Simposio de Computación Ubicua e Inteligencia Ambiental, UCAmI 2005*. 13/09/2005.

Moll, F. **Wearable bluetooth communications powered by energy harvesting techniques**. *I Simposio de Computación Ubicua e Inteligencia Ambiental, UCAmI 2005*. 13/09/2005.

Moll, F. **MEASUREMENT OF MULTIPLE CROSSTALK-INDUCED DELAY IN A SUBMICRON TECHNOLOGY**. *XIV Design of Circuits and Integrated Systems Conference*. 16/11/1999.

Moll, F. **Extraction of Equivalent Circuit models of package power supply distribution systems from full wave EM simulations**. *IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging*. 26/10/1998.

Moll, F. **Analysis and measurement of the behaviour of a latch in the presence of spurious signals**. *XI Design of Integrated Circuits and Systems Conference*. 20/11/1996.

Moll, F. **Detectability of spurious signals with limited propagation in combinationa]..**. *ATS 94. Asian Test Symposium*. 15/11/1994.

Moll, F. **Analysis of Parasitic Coupling in Distributed Parameter Lines**. *PATMOS 93. Power and timing modeling for performace of integrated*. 11/10/1993.

Moll, F. **Methodology of detection of spurious signals in VLSI circuits**. *ETC 93 European Test Conference*. 19/04/1993.

B.2 Imparting courses

B.3 Provide of conference

B.4 Participation in exhibitions

B.5 Organization of conferences

Member of the organising committee: XXXII Conference on Design of Circuits and Integrated Systems. Barcelona, Espanya. 2017.

Secretary of the organising committee: Variability modelling and mitigation techniques in current and future technologies. Dresden, Germany. 2012.

B.6 Organization of courses and seminars

Organitzador Principal: Variation tolerant circuit design, impartida per Kaushik Roy de la Purdue University, USA. 2009. Barcelona.

B.7 Organisation of award ceremonies

B.8 Membership of conference organising committees

Member. **Steering Committee**: *37th Conference on Design of Circuits and Integrated Systems*. Pamplona, Espanya. 01/12/2021 - 30/11/2022.

Member. **Steering Committee**: *36th Conference on Design of Circuits and Integrated Systems*. Vila do Conde, Portugal. 01/12/2020 - 30/11/2021.

Member. **Steering Committee**: *XXXV Conference on Design of Circuits and Integrated Systems*. Segovia, Espanya. 01/12/2019 - 30/11/2020.

Member. **Steering Committee**: *XXXIII Conference on Design of Circuits and Integrated Systems*. Lyon, France. 01/12/2017 - 30/11/2018.

Member. **Technical Program Committee - Topic D5: Power Estimation and Optimization**: *Design, Automation & Test in Europe Conference & Exhibition*. Grenoble, France. 01/09/2012 - 01/09/2012.

Other. **Comitè de la edició del congres I Simposio de Computación Ubicua e Inteligencia Ambiental, UCAmI 2005**: *I Simposio de Computación Ubicua e Inteligencia Ambiental, UCAmI 2005*. Granada, Espanya. 13/09/2005 - 13/09/2005.

B.9 Attendance at course or seminar

Introduction to Sustainability in Electronics (GreenChips-EDU Project). Barcelona, Espanya. 2024.

En què consisteix l'anàlisi de sostenibilitat del TFG/TFM - 3a. edició PRESENCIAL - Campus Nord. Barcelona, Espanya. 2024.

Metodologies àgils com a eines per a la millora del treball en equip, la planificació i gestió de projectes.. Barcelona, Espanya. 2019.

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Direcció de treballs de fi de grau i màster. Barcelona, Espanya. 2014.

C. Projects and intellectual and industrial property

C.1 Participation in R&D calls

Researcher. **Chips para arquitecturas avanzadas y sistemas fotónicos**. Scientific coordinator: Rubio, A.. 12/09/2023 - 30/06/2026. Duration: 02 year/s 09 month/s 19 day/s . Funding: 3.761.798,45 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: MIN DE ECONOMIA Y COMPETITIVIDAD.

Researcher. **Efficient and Robust Integrated Circuits and Systems**. Scientific coordinator: Rodriguez-Montanes, R.. 01/01/2022 - 30/06/2025. Duration: 03 year/s 06 month/s . Funding: 0,00 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

Researcher. **The variability challenge in nano-cmos and beyond-cmos: novel ic design paradigms for mitigation and exploitation**. Scientific coordinator: Rodriguez-Montanes, R.; Rubio, A.. 01/06/2020 - 29/02/2024. Duration: 03 year/s 09 month/s . Funding: 193.600,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: AGENCIA ESTATAL DE INVESTIGACION.

Scientific coordinator. **Investigación, formación y prospectiva en sistemas RISC-V**. Scientific coordinator: Moll, F.; Canal, R.; Morancho, E.. 08/10/2019 - 07/10/2022. Duration: 03 year/s . Funding: 25.000,00 €. Scope: National. Institution in which the research was undertaken: Barcelona Microelectronics Institute. Funding body: MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES.

Scientific coordinator. **001-P-001723_Disseny d'acceleradors basats en la tecnologia RISC per a la propera generació de computadors (DRAC)**. Scientific coordinator: Moll, F.. 01/06/2019 - 31/12/2022. Duration: 03 year/s 07 month/s . Funding: 5.539,89 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: GENCAT - DEPT. D'EMPRESA I OCUPACIO.

Scientific coordinator. **001-P-001723_Disseny d'acceleradors basats en la tecnologia RISC per a la propera generació de computadors (DRAC)**. Scientific coordinator: Moll, F.. 01/06/2019 - 31/12/2022. Duration: 03 year/s 07 month/s . Funding: 33.239,33 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: GENCAT - DEPT. D'EMPRESA I OCUPACIO.

Scientific coordinator. **001-P-001723_Disseny d'acceleradors basats en la tecnologia RISC per a la propera generació de computadors (DRAC)**. Scientific coordinator: Moll, F.. 01/06/2019 - 31/12/2022. Duration: 03 year/s 07 month/s . Funding: 55.398,89 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: GENCAT - DEPT. D'EMPRESA I OCUPACIO.

Scientific coordinator. **001-P-001723_Disseny d'acceleradors basats en la tecnologia RISC per a la propera generació de computadors (DRAC)**. Scientific coordinator: Moll, F.. 01/06/2019 - 31/12/2022. Duration: 03 year/s 07 month/s . Funding: 16.619,66 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: GENCAT - DEPT. D'EMPRESA I OCUPACIO.

Scientific coordinator. **Towards Trusted Low-Power Things: Devices, Circuits and Architectures**. Scientific coordinator: Rubio, A.; Moll, F.. 30/12/2016 - 29/06/2021. Duration: 04 year/s 06 month/s . Funding: 243.815,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: MIN DE ECONOMIA Y COMPETITIVIDAD.

Researcher. **Multilevel approach to the reliability-aware design of analog and digital integrated circuits**. Scientific coordinator: Rubio, A.; Mateo, D.. 01/01/2014 - 31/12/2018. Duration: 05 year/s . Funding: 261.481,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: MIN DE ECONOMIA Y COMPETITIVIDAD.

Researcher. **Terascale reliable adaptive memory systems**. Scientific coordinator: Rubio, A.. 01/01/2010 - 31/12/2012. Duration: 03 year/s . Funding: 413.066,50 €. Scope: European. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Commission of European Communities.

Researcher. **Principios de diseño y test de sistemas integrados en tera-escala**. Scientific coordinator: Rubio, A.. 01/12/2009 - 30/11/2013. Duration: 04 year/s . Funding: 0,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Ministerio de Ciencia e Innovación.

Scientific coordinator. **Synthesis using advanced process technology integrated in regular cells, IPs, architectures, and design platforms**. Scientific coordinator: Moll, F.. 02/11/2009 - 03/02/2013. Duration: 03 year/s 03 month/s 02 day/s . Funding: 337.638,00 €. Scope: European. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Commission of European Communities.

Researcher. **GRUP DE RECERCA DE CIRCUITS I SISTEMES INTEGRATS D'ALTES PRESTACIONS (HIPICS)**. Scientific coordinator: Aragones, X.. 22/07/2009 - 30/04/2014. Duration: 04 year/s 09 month/s 09 day/s . Funding: 44.720,00 €. Scope: Regional. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: AGAUR. Agència de Gestió d'Ajuts Universitaris i de Recerca.

Scientific coordinator. **Modeling and design of reliable, process-variation aware nanoelectronic devices,circuits and systems**. Scientific coordinator: Moll, F.. 01/04/2009 - 31/03/2012. Duration: 03 year/s . Funding: 173.363,00 €. Scope: European. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Ministerio de Ciencia e Innovación (MICINN).

Scientific coordinator. **Modeling and design of reliable, process-variation aware nanoelectronic devices,circuits and systems**. Scientific coordinator: Moll, F.. 01/03/2009 - 28/02/2012. Duration: 02 year/s 11 month/s 28 day/s . Funding: 33.953,98 €. Scope: European. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Commission of European Communities.

Researcher. **Design And Test Principles For Terascale Integrated Systems**. Scientific coordinator: Rubio, A.. 01/01/2009 - 31/12/2013. Duration: 05 year/s . Funding: 551.155,00 €. Scope: National. Institution in which the research was undertaken: Departament d'Enginyeria Electrònica-UPC. Funding body: Gobierno de España. Ministerio de Ciencia e Innovación (Micinn).

Researcher. **PRINCIPIOS DE DISEÑO Y TEST DE SISTEMAS INTEGRADOS EN TERA-ESCALA**. Scientific coordinator: Rubio, A.. 01/01/2009 - 30/06/2014. Duration: 05 year/s 06 month/s . Funding: 548.779,80 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Ministerio de Ciencia e Innovación (MICINN).

Researcher. **Sistema integrado en chip (SoC) de muy bajo consumo para redes inalámbricas ad-hoc**. Scientific coordinator: Aragones, X.. 13/12/2004 - 12/12/2005. Duration: 01 year/s . Funding: 17.020,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: Gobierno de España. Ministerio de Ciencia y Tecnología. Secretaría de Estado de Política Científica y Tecnológica.

Researcher. **Modelación de acoplamientos parásitos en circuitos integrados, aplicación a diseño digital de bajo nivel de ruido y altas prestaciones**. Scientific coordinator: Rubio, A.. 01/01/1996 - 31/01/1998. Duration: 02 year/s 01 month/s 01 day/s . Funding: 100.000,00 €. Scope: National. Institution in which the research was undertaken: Department of Electronic Engineering. Funding body: CICYT.

C.2 Participation in non-competitive R&D projects

Scientific coordinator. **SISTEMA AUTÒNOM DE COMANDAMENT D'ELEMENTS**. Scientific coordinator: Moll, F.. 10/06/2003 - 26/11/2003. Duration: 05 month/s 19 day/s . Funding: 9.300,00 €. Institution in which the research was undertaken: Department of Electronic Engineering.

C.3 Participation in teaching innovation projects

C.4 Industrial and intellectual property rights

Calomarde, A.; Rubio, A.; Moll, F.; García, L. **Procedimiento para la mejora de la fiabilidad de circuitos integrados digitales en condiciones de baja relación señal a ruido**. Brief description: Procedimiento para la mejora de la fiabilidad de circuitos integrados digitales en condiciones de baja relación señal a ruido. Procedimiento para la mejora de la fiabilidad de circuitos integrados digitales en condiciones ambientales no favorables, o con tecnologías con dificultades de fabricación o bajo rendimiento, cuyos componentes son imperfectos. El procedimiento permite mejorar la fiabilidad de funcionamiento bajo condiciones adversas, tales como ruido, bajo nivel de alimentación, etc., mediante el uso de realimentación local de una serie de nodos seleccionados.. Registration number: **P200901626**. **Invention patent**. Date of registration: 15/07/2009. Country of registration: Espanya. Scope: National. Property-holding institution: Universitat Politècnica de Catalunya.

Rubio, A.; Moll, F.; Gonzalez, J.; Roselló, A.; Martorell, F. **Sistema para el control de la distancia de un conjunto de elementos a un elemento de referencia**. Registration number: **200300385**. **Invention patent**. Date of registration: 01/09/2004. Country of registration: Espanya. Scope: International. Property-holding institution: Antonio Rosello Junyent.

Altet, J.; Aragones, X.; Gonzalez, J.; Mateo, D.; Moll, F.; Rubio, A. **Procedimiento de verificación estructural de circuitos analógicos basado en la observación interna y concurrente de temperatura**. Registration number: **P200002735**. **Invention patent**. Date of registration: 03/11/2000. Country of registration: Espanya. Scope: National. Property-holding institution: UPC.

C.5 Software

D. Products

D.1 Datasets

E. Committees and societies

E.1 Membership of advisory or assessment committees

Reviewer. **ANR - Agence Nationale de la Recherche (Agència Nacional Francesa de Recerca)**. 01/11/2014

E.2 Membership of award panel or jury

E.3 Membership of architecture competition panel or jury

E.4 Membership of scientific societies

Member. **IEEE, Institute of Electric and Electronic Engineers**. 01/10/1993

Member. **Institute of Electrical and Electronics Engineers**. Institute of Electrical and Electronics Engineers. 01/01/1993

Member. **APS, American Physical Society**. 01/01/1992 - 01/01/1999.

F. Contributions to publications and theses

F.1 Contributions to journals

Reviewer: **Journal of electronic testing. Theory and applications**. 01/11/2010

Reviewer: **Electronics letters**. 09/11/2003

Reviewer: **International journal of electronics**. 02/01/2000

Reviewer: **IEE proceedings-Circuits devices and systems**. 01/06/1997

F.2 Contributions to books

F.3 Contributions in the media

F.4 Supervision or tutoring of theses and membership of assessment panels

Supervisor , Secretari. Work author: **Lostes, O.** ***Smough: Design and evaluation of an heterogeneous architecture for large genome sequence alignment.*** **Treball de fi de màster**. 31/10/2024. Mark: Excellent. Supervisor/s: Doblas, M.; Moll, F.. Universitat Politècnica de Catalunya.

President. Work author: **Ruiz Escudero, Alejandro.** ***Disseny d?un convertidor Analògic Digital de baix consum i baixa àrea en una tecnologia CMOS de 65nm.*** **Bachelor's thesis**. 29/10/2024. Mark: Very Good. Supervisor/s: Mateo, D.; Altet, J.. Universitat Politècnica de Catalunya.

President. Work author: **Souto Ruiz, Paula.** ***RISC-V Based Low-Latency Communication Accelerator for automotive Applications.*** **Bachelor's thesis**. 29/10/2024. Mark: Excellent. Supervisor/s: Moreno, J.; Blanch, M.. Universitat Politècnica de Catalunya.

President. Work author: **Zhu Wang, Shexing.** ***Architecture, RTL implementation and verification of the MIPI CSI-2/D-PHY transmitter version 1.2/1.3.*** **Treball de fi de màster**. 13/09/2024. Mark: A with honours. Supervisor/s: Mateo, D.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Oliete Escuin, Noelia.** ***PEACH: Pattern Exact-Matching Acceleration with a near CPU Hardware Learned Index Engine.*** **Treball de fi de màster**. 13/09/2024. Mark: Excellent. Supervisor/s: Alvarez, L.; Moll, F.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Rodríguez Gracia, Juan Antonio.** ***Evaluation of different acceleration techniques applied to the Dilithium post-quantum cryptography algorithm.*** **Treball de fi de màster**. 12/09/2024. Mark: Excellent. Supervisor/s: Carril Gil, X.; Moll, F.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Riatti, Chiara.** ***Design and Implementation of Instruction Fusion Techniques in a RISC-V Out-Of-Order core.*** **Treball de fi de màster**. 12/09/2024. Mark: A with honours. Supervisor/s: Moll, F.; Mendoza, J.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Moreno Martín viveros, Álvaro.** ***Analysis of a reuse-driven L0 data cache inside a RISCV high-performance computing system.*** **Treball de fi de màster**. 09/09/2024. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Grau I fornt, Marc.** ***Development of the Lockstep Version of the Sargantana RISC-V Core.*** **Treball de fi de màster**. 15/07/2024. Mark: Excellent. Supervisor/s: Abella Ferrer, Jaime; Moll, F.. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Arnaiz, D.** ***Bringing Self-Awareness to the Extreme Edge - A Distributed Approach for Adaptive Energy Management in WSNs Applied to Structural Health Monitoring.*** **Doctoral thesis**. 02/07/2024. Mark: Excellent. Supervisor/s: Alarcon, E.; Vilajosana, X.; Moll, F.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Fontanet Albinyana, Bernat.** ***Fusion of 2D and 3D sensor data for autonomous driving.*** **Bachelor's thesis**. 27/05/2024. Mark: Excellent. Supervisor/s: Casas, J.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Matas Enjuanes, Joan.** ***Generation of differentially private trajectories with machine learning.*** **Bachelor's thesis**. 27/05/2024. Mark: Excellent. Supervisor/s: Parra-Arnau, J.; Forne, J.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Escudé Pujol, Manuel.** ***Fitació superior taxa d'informació d'estructures en esquemes per compartir secrets: algorismes combinatoris.*** **Bachelor's thesis**. 27/05/2024. Mark: Excellent. Supervisor/s: Saez, G.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **El Mehtar garcía, Sarah.** ***Implementation of a DDR3 PHY in a 22nm***

technology. **Treball de fi de màster**. 13/05/2024. Mark: A with honours. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Ponent, Secretari. Work author: **Brahimllari, Klea.** ***Physical implementation and verification of a multi-phase clock system.*** **Treball de fi de màster**. 08/05/2024. Mark: Excellent. Supervisor/s: Giaccone, L.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Rodas Quiroga, Narcís.** ***Integration of a vector processing unit in a dual-issue out-of-order RISC-V processor.*** **Treball de fi de màster**. 05/02/2024. Mark: Excellent. Supervisor/s: Moll, F.; Moreto, M.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Molina-Burgués, R.** ***SIMPLE RANDOMIZED STRATEGIES FOR LOW-RANK MATRIX COMPRESSION.*** **Treball de fi de màster**. 11/01/2024. Mark: Excellent. Supervisor/s: Rius, J.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Bigas Soldevila, Arnau.** ***Integration of a High Performance Cache with a RISC-V Core and Cost-Benefit Analysis.*** **Treball de fi de màster**. 31/10/2023. Mark: Excellent. Supervisor/s: Moll, F.; Alvarez, L.. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Rodríguez Tortajada, Miquel.** ***Evaluation of open-source synthesis tools for ASIC Design.*** **Bachelor's thesis**. 20/10/2023. Mark: Very Good. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Palma, K.** ***Exploration of FDSOI Back-Biasing Techniques to Hinder Cryptographic Attacks Based on Leakage Current.*** **Doctoral thesis**. 18/10/2023. Mark: Excellent Cum Laude. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya. <http://hdl.handle.net/10803/690282> .

Secretari, Supervisor . Work author: **Albort Vergés, Sergi Xabier.** ***Implementation of a deep learning accelerator in an open-source PDK.*** **Treball de fi de màster**. 12/09/2023. Mark: Excellent. Supervisor/s: Fornt, J.; Moll, F.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Pereira Dos santos, Victor Jerri.** ***Team Recognition in Sports Events.*** **Treball de fi de màster**. 07/09/2023. Mark: Excellent. Supervisor/s: Marques, F.; Rius Ferrer, Ignasi. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Torrubia Ollero, Alex.** ***Efficient implementation of a Content-Addressable Memory in a 22nm technology.*** **Treball de fi de màster**. 07/09/2023. Mark: Excellent. Supervisor/s: Figueras, R.; Moll, F.. Universitat Politècnica de Catalunya.

President. Work author: **López Guillén, Alberto.** ***Design of a rail-to-rail OTA in 65 nm CMOS technology for a particle detector sensor.*** **Treball de fi de màster**. 13/07/2023. Mark: Excellent. Supervisor/s: Aragones, X.; Picatoste, E.. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Fornt, J.** ***Designing Deep Learning Accelerators in the limits of Energy Efficiency.*** **Pla de recerca**. 06/07/2023. Mark: Satisfactory. Supervisor/s: Moll, F.; Altet, J.; Moll, F.. Universitat Politècnica de Catalunya.

Secretari. Work author: **Peris Ponferrada, Alex.** ***Disseny d'una resistència activa per a un circuit integrador en 65 nm per a capturar el Night Sky Background en observatoris Cherenkov Telescope Array.*** **Bachelor's thesis**. 03/07/2023. Mark: Very Good. Supervisor/s: Mateo, D.; Aragones, X.; Gomez, S.. Universitat Politècnica de Catalunya.

Secretari. Work author: **Martínez Domingo, Sergio.** ***Self compensation of Aging in Integrated Circuits using***

built-in temperature measurements.. **Bachelor's thesis**. 03/07/2023. Mark: Excellent. Supervisor/s: Altet, J.; Mateo, D.. Universitat Politècnica de Catalunya.

Secretari. Work author: **Galeano Pérez, Diego.** ***Design of a Digital Activation Function Unit for Neural Network Acceleration.*** **Bachelor's thesis**. 03/07/2023. Mark: Excellent. Supervisor/s: Altet, J.; Fornt, J.. Universitat Politècnica de Catalunya.

Secretari. Work author: **Cerro Miñana, Carlos.** ***Design of a Voltage Controlled Delay line using a 65nm CMOS technology.*** **Bachelor's thesis**. 03/07/2023. Mark: Very Good. Supervisor/s: Mateo, D.; Altet, J.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Ribalda Gálvez, Miquel.** ***Design of a Resistive RAM with asynchronous self-adaptive compensation for memristor variability on 130nm technology.*** **Treball de fi de màster**. 31/05/2023. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Aguiló Domínguez, David.** ***Physical design of a RISC-V processor with accelerators chip in 22nm FDSOI technology.*** **Treball de fi de màster**. 07/02/2023. Mark: Excellent. Supervisor/s: Moll, F.; Alonso, O.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Carril I gil, Xavier.** ***Design, Implementation and Evaluation of Post-Quantum Cryptography Accelerators in 22nm FDSOI technology.*** **Treball de fi de màster**. 02/02/2023. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

President. Work author: **Pautasso, Gianluca.** ***Design of a digital multi-precision multiply-accumulate unit.*** **Treball de fi de màster**. 13/09/2022. Mark: Excellent. Supervisor/s: Altet, J.. Universitat Politècnica de Catalunya.

President. Work author: **Olivé I muñiz, Marçal.** ***Experimental characterization of Random Telegraph Noise in FDSOI technology and its application for security primitives.*** **Treball de fi de màster**. 15/07/2022. Mark: Excellent. Supervisor/s: Aragones, X.; Mateo, D.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Codina I vilanova, Pol.** ***Implementation feasibility of an integrated LPDDR4 PHY block.*** **Treball de fi de màster**. 12/07/2022. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Bas Jalón, Francisco.** ***Design of a diversity enforcement module for safety critical processing systems.*** **Treball de fi de màster**. 12/07/2022. Mark: A with honours. Supervisor/s: Moll, F.; Abella Ferrer, Jaime. Universitat Politècnica de Catalunya.

Secretari. Work author: **Cisneros, J.** ***Low-Power High-Channel-Count CMOS ROICs for Multiplexed Arrays of Graphene Transistors in Large-Area µECoG.*** **Doctoral thesis**. 07/07/2022. Mark: Excellent. Supervisor/s: Guimera, A.; Aragones, X.; Serra-Graells, F.. Universitat Politècnica de Catalunya. <https://www.tdx.cat/handle/10803/183> .

Supervisor . Work author: **Jin, Leixin.** ***Impact of using approximate FP multipliers in a neural network.*** **Bachelor's thesis**. 25/05/2022. Mark: Excellent. Supervisor/s: Altet, J.; Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Doblas, M.** ***RISC-V core optimization in 22nm FD-SOI technology.*** **Treball de fi de màster**. 29/10/2021. Mark: Excellent. Supervisor/s: Moll, F.; Moreto, M.. Universitat Politècnica de Catalunya.

President. Work author: **Alcubilla Ayestaran, Mikel.** ***Hardware acceleration for real time processing systems.*** **Treball de fi de màster**. 09/07/2021. Mark: Very Good. Supervisor/s: Altet, J.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Palacio García, Héctor.** ***GEOSAR permanent continental observation. Impact of atmospheric and surface decorrelation.*** **Treball de fi de màster**. 08/07/2021. Mark: Excellent. Supervisor/s: Broquetas, A.. Universitat Politècnica de Catalunya.

Vocal. Work author: **Carrera Escalé, Pol.** ***Microwave filtering amplifiers.*** **Treball de fi de màster**. 07/07/2021. Mark: Excellent. Supervisor/s: Pradell, L.. Universitat Politècnica de Catalunya.

President. Work author: **Brahimllari, Eda.** ***Fully Automation of RTL architecture, DV environment and Physical Design flow constraints.*** **Treball de fi de màster**. 28/05/2021. Mark: Very Good. Supervisor/s: Aragones, X.. Universitat Politècnica de Catalunya.

Secretari. Work author: **Aymerich, J.** ***Low-Power Read-Out Ics for Smart Electrochemical Sensors.*** **Doctoral thesis**. 18/03/2021. Mark: Excellent Cum Laude. Supervisor/s: Aragones, X.; Dei, Michele; Serra-Graells, F.. Universitat Politècnica de Catalunya. <http://hdl.handle.net/10803/671918> .

Supervisor . Work author: **Safadi, H.** ***Design of a clock and data recovery circuit in FDSOI technology for high speed serial links.*** **Treball de fi de màster**. 12/03/2021. Mark: Excellent. Supervisor/s: Mateo, D.; Moll, F.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Subias Farreres, Ricard.** ***Physical implementation of an industrial design using a 180nm technology.*** **Treball de fi de màster**. 05/02/2021. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Fontova Musté, Pau.** ***Design for Testability methodologies applied to a RISC-Vprocessor.*** **Treball de fi de màster**. 05/02/2021. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Montabes Jiménez, Víctor Manuel.** ***Impact of physical low power techniques in a RISC-V processor.*** **Treball de fi de màster**. 04/02/2021. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Secretari, Supervisor . Work author: **Etxezarreta Martinez, Imanol.** ***Approximate arithmetic units under voltage under-scaling.*** **Treball de fi de màster**. 04/02/2021. Mark: Excellent. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Sala I sucarrats, Oriol.** ***Design and implementation of a traffic injector for a bus-based space multicore.*** **Treball de fi de màster**. 04/02/2021. Mark: Excellent. Supervisor/s: Moll, F.; Abella Ferrer, Jaime. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Martinez Buil, Paula.** ***Design of an Output Interface for an In-Memory-Computing CNN Accelerator.*** **Treball de fi de màster**. 27/11/2020. Mark: Excellent. Supervisor/s: Aragones, X.; Moll, F.. Universitat Politècnica de Catalunya.

Supervisor , Secretari. Work author: **Echeverria Olaiz, Unai.** ***In-Memory-Computing CNN Accelerator Employing Charge-Domain Compute.*** **Treball de fi de màster**. 26/11/2020. Mark: Excellent. Supervisor/s: Moll, F.; Aragones, X.. Universitat Politècnica de Catalunya.

Supervisor . Work author: **Nunes, D.** ***Ultra-low Power Circuits based on Tunnel FETs for Energy Harvesting Applications.*** **Doctoral thesis**. 19/05/2017. Mark: Excellent Cum Laude. Supervisor/s: Moll, F.; Valtchev, Stanimir. Universitat Politècnica de Catalunya. <http://hdl.handle.net/2117/108502> .

Supervisor . Work author: **Mauricio, J.** ***Monitor amb control strategies to reduce the impact of Process***

Variations in digital circuits. **Doctoral thesis**. 14/12/2015. Mark: Excellent Cum Laude. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya. <http://hdl.handle.net/10803/336374> .

Supervisor . Work author: **Gomez, S.** ***Regular Cell Design Approach Considering Lithography-Induced Process Variations.*** **Doctoral thesis**. 17/10/2014. Mark: Excellent Cum Laude. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya. <http://hdl.handle.net/10803/284205> .

Supervisor . Work author: **Pons, M.** ***Layout Regularity for Design and Manufacturability.*** **Doctoral thesis**. 02/10/2012. Mark: Pass. Supervisor/s: Moll, F.; Abella, J.. Universitat Politècnica de Catalunya. <http://www.tdx.cat/handle/10803/96983> .

Supervisor . Work author: **Mateu, M.** ***Energy harvesting from human passive power.*** **Doctoral thesis**. 05/06/2009. Mark: Excellent Cum Laude. Supervisor/s: Moll, F.. Universitat Politècnica de Catalunya. <http://hdl.handle.net/10803/48637> .

G. Personal acknowledgements

G.1 Awards and acknowledgements

G.2 Publications about the work

G.3 Architecture competitions

G.4 Grants

Moll, F. **Subprograma de Estancias de Investigadores españoles en centros de investigacion extranjeros**. MEC. 31/08/1997. Amount: 12.020,24 €.

G.5 Scholarships

G.6 Stretches of research, teaching and management

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2024.

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2019.

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2014.

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2009.

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2003.

z1. Universitat Politècnica de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2000.

z2. Number of segments recognized: 1. Date of acknowledgement: 01/01/2023.

z2. Number of segments recognized: 1. Date of acknowledgement: 01/01/2017.

z2. Number of segments recognized: 1. Date of acknowledgement: 01/01/2011.

z2. Number of segments recognized: 1. Date of acknowledgement: 01/01/2005.

z2. Number of segments recognized: 1. Date of acknowledgement: 01/01/2000.

z3. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2019.

z3. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2014.

z3. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2008.

z3. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2003.

z3. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2002.

z4. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2017.

z4. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2011.

z4. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2005.

z4. AQU - Agència de la Qualitat Universitària de Catalunya. Number of segments recognized: 1. Date of acknowledgement: 01/01/2003.

G.7 Accreditations

ACREDITACIÓ CU, ANECA. Awarding body: Agencia Nacional de Evaluación de la Calidad y Acreditación (ANECA). 22/06/2016.

G.8 Other merits

H. Stays and other activities

H.1 Stays in R&D centers

Post-doctoral . State University of new York at Binghamton. Purpose: Research. Comparable tasks: Estudi de modelació electromagnètica d'encapsulats electrònics. 01/02/1998 - 31/07/1998.

H.2 R&D management

H.3 Other activities

I. Teaching activities

I.1 Subject taught

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 2006.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2006.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 2005.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2005.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 2004.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2004.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 2003.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2003.

CIRCUITS I SISTEMES ELECTRÒNICS II. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2002.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 2002.

DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2002.

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DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 2000.

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DISSENY DE CIRCUITS I SISTEMES ELECTRO.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 1997.

CIRCUITS I SISTEMES ELECTRÒNICS II. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1996.

DISSENY DE CIRCUITS I SISTEMES ELECTR.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 1996.

DISSENY DE CIRCUITS I SISTEMES ELECTR.. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1996.

CIRCUITS I SISTEMES ELECTRÒNICS II. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1995.

DISSENY DE CIRCUITTS I SIST. ELECTRÒNICS. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 1995.

DISSENY DE CIRCUITTS I SIST. ELECTRÒNICS. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1995.

DISSENY DE CIRCUITTS I SIST. ELECTRÒNICS. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 1994.

DISSENY DE CIRCUITTS I SIST. ELECTRÒNICS. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1994.

CIRCUITS I SISTEMES ELECTRÒNICS I. Credits: 6.0. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. segon. 1993.

ELECTRÒNICA I. Degree: **Ingeniería en Telecomunicación**. Universitat Politècnica de Catalunya. **UPC**. primer. 1992.

I.2 Coordination teaching

I.3 Tutoring teaching

J. Scientific career summary and contribution relevant

J.1 Scientific career summary

Francesc Moll Echeto received the title of Bachelor of Physical Sciences from the Universitat de les Illes Balears in 1990 and the title of Doctor of Physical Sciences from the Universitat Politècnica de Catalunya in 1995. Since 1993 he has been associated as professor and researcher at the Electronic Engineering Department of the Universitat Politècnica de Catalunya in the area of Electronic Technology, taking up the position of University Professor (Titular de Universidad) in February 1997, a position he currently holds. Since 2022 he has been assigned as a researcher at the Barcelona Supercomputing Center/Centro Nacional de Supercomputación, where he is the group leader of the Synthesis and Physical Design of ICs group. His research activity has always been related to the design of integrated circuits and the effect of new technologies on the design and behavior of microelectronic circuits. During the training stage and the first years of his research career between 1990 and 2000 the central theme was the study of noise and couplings in chip and package interconnections, with participation in several projects of the Spanish Plan Nacional and a stay at the University of Binghamton (State University of New York) with professor Jiayuan Fang on electromagnetic modeling of encapsulates (year 1998). Around 2000 he began researching environmental energy recovery systems for very low consumption circuits, a line that proved very fruitful in publications and led to the direction of a doctoral thesis in 2009 (Loreto Mateu). In this area and in a second stage between 2014 and 2017 the study focused on the design of DC/DC converters with TFET devices aimed at very low voltage systems, an activity that led to the direction of a doctoral thesis in 2017 (David Cavalheiro). Around 2009, a new line of research began focusing on the study of process variability and design techniques to minimize its impact, which has continued with evolutions until today. In the first stage the research focused on the most technological aspects, with participation in three European projects (SYNAPTIC, MODERN TRAMS). At TRAMS, beyond-CMOS technologies (graphene transistors) began to be studied in addition to conventional CMOS technology. At SYNAPTIC the research focus was the study of regular layout design techniques in CMOS technologies. In these projects it was possible to collaborate with leading companies, such as Intel Labs Barcelona and STmicroelectronics. This first stage gave rise to two doctoral theses, in 2012 (Marc Pons) and 2014 (Sergio Gómez). In relation to the mitigation of variability, the design with FDSOI technology began to be studied and specifically the use of the polarization of the substrate (body biasing) as a variability mitigation technique, a line that will continue until 2023. This line gave rise to a doctoral thesis in 2015 (Joan Mauricio) and it evolved to focus the study on the possibility of using body biasing as a method to hinder attacks on cryptographic systems, with another doctoral thesis read in 2023 (Kenneth Palma). Likewise, in line with the research group, there has been work on memristor devices and their use to implement computing systems, participating in several projects of the Plan Nacional and giving rise to several publications. In 2018, a collaboration begins with the Barcelona Supercomputing Center for the CMOS design of advanced digital processors, initially within the framework of the DRAC project funded by the Generalitat de Catalunya to carry out the implementation in silicon of RISC-V processors and accelerators using 65nm and 22nm FDSOI technologies. This line has led to the assignment as a researcher in this center and the participation in several international projects, extending to this day: DRAC, eProcess, European Processor Initiative SGA1 and SGA2, and EUPilot. In all these areas he has participated in the publication of 37 indexed journals and more than 90 publications in conference proceedings. He has participated as a collaborating researcher since 1992 uninterruptedly in projects of the Plan Nacional in the area of ¿¿Information and Communication Technologies and Electronics and Communication Technologies. He has also acted as the representative of the UPC in the European microelectronics network Aeneas and in Europractice. Between March 2018 and September 2023, he held the position of coordinator of the UPC's Electronic Engineering doctoral program. Francesc is a Senior Member of the IEEE, a member of the Circuits and Systems and Solid State Circuits societies of the IEEE. From 2022 until the end of 2023 he held the position of Secretary of the Spanish Chapter of Circuits and Systems of the IEEE. Between January 2024 and December 2026, he holds the position of president of the Spanish Chapter of Circuits and Systems of the IEEE.

J.2 Contribution relevant