CURRICULUM VITAE ABREVIADO (CVA)

IMPORTANT – The Curriculum Vitae cannot exceed 4 pages. Instructions to fill this document are available in the website.

Part A. PERSONAL INFORMATION

First name	ALEJANDRO		
Family name	LINARES BARRANCO		
Gender (*)	MALE	Birth date (dd/mm/yyyy)	
Social Security, Passport, ID number			
e-mail	alinares@us.es	https://prisma.us.es/investigador/2199	
Open Researcher and Contributor ID (ORCID)		0000-0002-6056-740X	

A.1. Current position

Position	Professor (Catedrático de Universidad)		
Initial date	10/Jun/2021		
Institution	University of Seville		
Department/Center	Architecture and Technology of Computers	Research Institute on Computer Engineering (I3US)	
Country	SPAIN	Teleph. number	+34954556145
Key words	Neuromorphic Engineering; Robotics; VLSI; FPGA; Real-time;		

A.2. Previous positions (research activity interuptions, indicate total months)

Period	Position/Institution/Country/Interruption cause
2009-2021	Associate Professor / University of Seville / Spain
2003-2009	Assistant Professor / University of Seville / Spain

A.3. Education

PhD, Licensed, Graduate	University/Country	Year
PhD on Industrial Informatics	University of Seville	2003
MSc on Industrial Informatics	University of Seville	2002
BSc on Computer Engineering	University of Seville	1998

Part B. CV SUMMARY *(max. 5000 characters, including spaces)*

CNEAI awards (sexenios): 4 Research awards for periods: 1999-2005, 2006-2011, 2012-2017, 2018-2023), 1 Knowledge Transfer award until the year 2015.
PhD advisor concluded thesis in the last 10 years: 6 (9 in total)
Number of papers at JCR-Q1: 21 (JCR), 29 (SJR) (https://prisma.us.es/investigador/2199)
Google Scholar (https://scholar.google.es/citations?user=oihgDkoAAAAJ&hl=es): 208 papers, 3980 cites (2005 since 2019), h-index: 32 (24 since 2019), i10: 78 (47 since 2019).
ResearchGate (https://www.researchgate.net/profile/Alejandro_Linares-Barranco): 215 papers, 48037 reads, 3135 cites, RIS=1402, (above 94% of researchers in this network).
ScopusID (http://www.scopus.com/authid/detail.url?authorId=8960244800): for 183 papers, 2494 cites from 1550 papers, h-index: 27.
ResearcherID (https://www.webofscience.com/wos/author/record/B-7087-2011): 164 papers until 2023 (Web of Science), 1890 cites and h-index of 23.
My research is focused on: Neuromorphic Engineering, co-design HW/SW embedded systems; microcontrollers & real-time OS; FPGAs; Event-driven Neuro-inspired systems (AER) and interfaces; Neuro-robotics; event-driven vision/audio processing; deep learning. I started my research in the European project CAVIAR in 2002 with the development of chip-to-chip / chip-to-computer interfaces for neuromorphic AER systems (PCB, VHDL, FPGA, microcontrollers, Java) and simulation tools for theoretical studies on the transformation of static images to AER format, the central focus of my doctoral thesis. This allowed me to perform several visits abroad, which resulted in numerous publications both in JCR-Q1

journals (IEEE, IEE, ELSEVIER, SPRINGER, …) and in multiple high-impact conferences (CORE & GRIIN databases). To date, the neuromorphic line has allowed me to serve as IP at an European project (SMALL), four projects of the Spanish R+D+i plan (VULCANO, BIOSENSE, COFNET, and MINDROB, mostly in partnership with IMSE), two Excellence projects of the Andalusian Government (MINERVA, DAFNE), one industrial transfer project (PROMETEO) and two international projects with private funding (Samsung Ltd.) from 2015 to 2020 (NPP and NPP2). These participations as IP and others as a researcher have allowed me to accumulate the publications and research merits expressed in this CVA. The PROFESSIONAL EXPERIENCE I had in SAINCO-ABENGOA in 1999-2000 (design of digital circuits in VHDL for FPGA and ASIC for Power Line communications stage) gave me perspective and experience for the development of my current research. In 2014 we created a Spinoff company of the Univ. of Seville (EBT COBER SL - www.t-cober.es) of which I am a partner and with which we manufacture robotic biomedical analysis instruments for VITRO SL, among other clients/activities. I have taught in the second cycle of computer engineering of the 1997 syllabuses, in the current degrees of Computer Engineering and Industrial Electronics Engineering (2010 syllabuses); master degrees of Computing, Computer and Network Engineering (until 2017), Computer Engineering, Biomedical Engineering and Digital Health, and Teaching Staff (MAES); and in the PhD programs of Industrial Informatics, Systems and Installations for Industry and at other universities such as UZH/ETHZ, Univ. Cádiz, Univ. Politécnica de Cartagena. I've done several research visits (three months or longer periods) to Bielefeld U., Ulster U. and Zurich U. I have directed more than 80 PFC, TFG, DEA, TFM, and 9 doctoral theses to date, where some of these students work at important companies in Germany, Switzerland and Italy, and others remain at Academia. Regarding MANAGEMENT in my university, I belong to several commissions of both the School and Department, including the quality of several degrees. I have served as SECRETARY of my dept (2013-2017) and as DIRECTOR (2017-2021). I am secretary of the doctoral program of Installations and Systems for the Industry since 2017. I have also served as IP at several collaboration agreements between several companies (national and foreign) and the Fidetia foundation, based in my School of Computer Engineering in Seville. These agreements have been oriented to internships in companies in some cases, to training of companies' personnel in others and to the transfer of knowledge with software and hardware applications for FPGA and microcontrollers, currently being exploited by third companies (for example Samsung, Intel, AERTEC, VITRO, McPuarsa, Synsense, Rexen, among others). As well as the production and tutoring of on-line training courses approved by the Junta de Andalucía and oriented to teachers. The Junta de Andalucía has recognized five research tranches for the "Complementos Autonómicos" in 2019.

Part C. RELEVANT MERITS *(sorted by typology)*

C.1. Publications *(see instructions): corresponding author. (nº x / nº y): position / total authors. SCOPUS (#citations). (AC) = corresponding author*

1. Schoepe, Thorben (AC); Gutiérrez-Galán, Daniel; Domínguez-Morales, Juan P.; Greatorex, Hugh; Jiménez-Fernández, Ángel; **Linares-Barranco, Alejandro**; Chicca, Elisabetta. (6/7). **2023**. Closed-loop sound source localization in neuromorphic systems. Neuromorphic Computing and Engineering. Vol 3. Num. 2. Pps 1-18. ISSN 2634-4386. SCOPUS (3) https://doi.org/10.1088/2634-4386/acdaba

2. Canas-Moreno, Salvador (AC); Piñero-Fuentes, Enrique; Ríos-Navarro, Antonio; Cascado-Caballero, Daniel; Pérez-Peña, Fernando; **Linares-Barranco, Alejandro**. (6/6). **2023**. Towards neuromorphic FPGA-based infrastructures for a robotic arm. AUTONOMOUS ROBOTS. SPRINGER. Vol 47. Pps. 947-961. ISSN 0929-5593, ISSN 1573-7527. SCOPUS (0) https://doi.org/10.1007/s10514-023-10111-x

3. Gutiérrez-Galán, Daniel (AC); Schoepe, Thorben; Domínguez-Morales, Juan P.; Jiménez-Fernández, Ángel; Chicca, Elisabetta; **Linares-Barranco, Alejandro**. (6/6). **2022**. An event-based digital time difference encoder model implementation for neuromorphic systems. IEEE TNNLS. Vol. 33. Num. 5, pp.1959-1973. ISSN 2162-2388. SCOPUS (6). https://doi.org/10.1109/TNNLS.2021.3108047

4. Gutiérrez-Galán, D. (AC); Domínguez-Morales, J. P.; Jiménez-Fernández, A.; **Linares-Barranco, A**.; Jiménez-Moreno, G.(4/5). **2021**. OpenNAS: Open Source Neuromorphic Auditory Sensor HDL code generator for FPGA implementations. NEUROCOMPUTING. ELSEVIER. Vol. 436. Pps. 35-38. ISSN 0925-2312. SCOPUS (6) https://doi.org/10.1016/j.neucom.2020.12.062

5. Linares-Barranco, Alejandro (AC); Pérez-Peña, Fernando; Jiménez-Fernández, Ángel; Chicca, Elisabetta. (1/4). **2020**. ED-BioRob: a neuromorphic robotic arm with FPGA-based infrastructure for bio-inspired spiking motor controllers. Frontiers in Neurorobotics. Vol. 14. Pps. 1-12. ISSN 1662-5218. SCOPUS (9) https://doi.org/10.3389/fnbot.2020.590163
6. Gutiérrez-Galán, Daniel (AC); Domínguez-Morales, J.P.; Pérez-Peña, Fernando; Jiménez-Fernández, Ángel; **Linares-Barranco, Alejandro**. (5/5). **2020**. Neuropod: a real-time neuromorphic spiking CPG applied to robotics. NEUROCOMPUTING. ELSEVIER. Vol. 381. Pps.10-19. ISSN 0925-2312. SCOPUS (29), https://doi.org/10.1016/j.neucom.2019.11.007
7. Tapiador-Morales, Ricardo (AC); **Linares-Barranco, Alejandro**; Jiménez-Fernández, Ángel; Jiménez-Moreno, Gabriel. (2/4). **2019**. Neuromorphic LIF Row-by-Row Multiconvolution Processor for FPGA. IEEE TBIOCAS. IEEE. Vol. 13-1. Pps.159-169. ISSN 1932-4545. SCOPUS (23), https://doi.org/10.1109/TBCAS.2018.2880012
8. Aimar, Alessandro (AC); Mostafa, Hesham; Calabrese, E.; et al; Delbruck, Tobi; **Linares-Barranco, Alejandro**. (9/11). **2019**. NullHop: A Flexible Convolutional Neural Network Accelerator Based on Sparse Representations of Feature Maps. IEEE TNNLS. IEEE. Vol.30. Pp.644-656. ISSN 2162-2388. SCOPUS (168), https://doi.org/10.1109/TNNLS.2018.2852335
9. Linares-Barranco, Alejandro; Pérez-Peña, Fernando; Moeys, Diederik Paul; Gómez-Rodríguez, Francisco; Jiménez-Moreno, Gabriel; Liu, Shih Chii; Delbruck, Tobi. (1/7). 2019. Low latency event-based filtering and feature extraction for dynamic vision sensors in real-time FPGA applications. IEEE ACCESS. IEEE. 7, pp.134926-134942. ISSN 2169-3536. SCOPUS (19), https://doi.org/10.1109/ACCESS.2019.2941282
10. Gutierrez-Galan, D.; Dominguez-Morales, Juan P.; Cerezuela-Escudero, E.; et al; **Linares-Barranco, A**.(9/9). 2018. Embedded neural network for real-time animal behavior classification. NEUROCOMPUTING. ELSEVIER. 272, pp.17-26. ISSN 0925-2312. SCOPUS (32), https://doi.org/10.1016/j.neucom.2017.03.090

C.2. Congress, indicating the modality of their participation (invited conference, oral presentation, poster)
1. Rios-Navarro, A.; Guo, S.; Abarajithan, G.; Vijayakumar, K.; **Linares-Barranco, A**.; Aarrestad, T.; Kastner, R.; Delbruck, T. Within-Camera Multilayer Perceptron DVS Denoising. **2023** (**Lecture**). IEEE Computer Society Conference on Computer Vision and Pattern Recognition Workshops (ISSN 2160-7508). CVPR. Vancouver-Canadá.
2. Rios-Navarro, A. ; Pinero-Fuentes, E.; Canas-Moreno, S.; Javed, A.; Harkin, J.; **Linares-Barranco, A**. LIPSFUS: A neuromorphic dataset for audio-visual sensory fusion of lip Reading. **2023** (**Lecture**) Proceedings - IEEE International Symposium on Circuits and Systems. ISSN 0271-4310. ISCAS. Monterey-CA. USA.
3. Piñero-Fuentes, E. ; Canas-Moreno, S.; Ríos-Navarro, A.; Cascado-Caballero, D.; Jiménez-Fernández, A.; **Linares-Barranco, A**. An MPSoC-based on-line edge infrastructure for embedded neuromorphic robotic controllers. **2022** (**Lecture**). Proceedings - IEEE International Symposium on Circuits and Systems. ISSN 0271-4310. ISCAS. Austin-TX. USA.
4. **Linares-Barranco, A**. ; Piñero-Fuentes, E.; Canas-Moreno, S.; Ríos-Navarro, A.; Maryada; Wu, Chenxi; Zhao, Jingyue; Zendrikov, D.; Indiveri, G. Towards hardware Implementation of WTA for CPG-based control of a Spiking Robotic Arm. **2022** (**Lecture**). Proceedings - IEEE International Symposium on Circuits and Systems. ISSN 0271-4310. ISCAS. Austin-TX. USA.
5. Tapiador-Morales, R.; Rios-Navarro, A.; Dominguez-Morales, J.P.; Gutierrez-Galan,
D.; **Linares-Barranco, A.**. Spiking row-by-row FPGA multi-kernel and multi-layer convolution processor. **2019** (**Lecture**). Proceedings - 29th International Conference on Field-Programmable Logic and Applications, FPL 2019. Barcelona-Spain.
6. Rios-Navarro, A.; Tapiador-Morales, R.; Jimenez-Fernandez, A.; Amaya, C.; Dominguez-Morales, M.; Delbruck, T.; **Linares-Barranco, A**.. Performance evaluation over HW/SW co-design SoC memory transfers for a CNN accelerator. 2018 (Lecture). 18TH International Conference On Nanotechnology (IEEE-NANO). Cork-Ireland.
7. Liu, Hongjie; Rios-Navarro, Antonio; Moeys, Diederik Paul; Delbruck, Tobi; **Linares-Barranco, Alejandro**. Neuromorphic Approach Sensitivity Cell Modeling and FPGA Implementation. **2017** (**Lecture**). Artificial Neural Networks And Machine Learning (ICANN). Best paper award. Alghero-Sardinia-Italy.
8. Berner, R ; Delbruck, T; Civit-Balcells, A; Linares-Barranco, A. A 5 meps $100 USB2.0 address-event monitor-sequencer interface. 2007 (Lecture). IEEE International Symposium On Circuits And Systems (ISCAS). SCOPUS (78). Orlando-FL. USA.

9. Gomez-Rodriguez, F ; Paz, R; **Linares-Barranco, A**; Rivas, M; Miro, L; Vicente, S; Jimenez, G; Civit, A. AER tools for communications and debugging. **2006** (**Lecture**). IEEE International Symposium On Circuits And Systems (ISCAS). SCOPUS (43). Kos-Greece.
10. Serrano-Gotarredona, R.; Oster, M.; Lichtsteiner, P.; **Linares-Barranco, A.**; Paz-Vicente, R.; Gómez-Rodríguez, F.; Kolle Riis, H.; Delbrück, T.; Liu, S. C.; Zahnd, S.; Whatley, A. M.; Douglas, R.; Häfliger, P.; Jimenez-Moreno, G.; Civit, A.; Serrano-Gotarredona, T.; Acosta-Jiménez, A.; Linares-Barranco, B. AER building blocks for multi-layer multi-chip neuromorphic vision systems. **2005** (**Lecture**). Advances in Neural Information Processing Systems (NIPS). SCOPUS (70). Vancouver-Canada.

C.3. Research projects, indicating your personal contribution. In the case of young researchers, indicate lines of research for which they have been responsible.
1. PID2019-105556GB-C33, Percepción y cognición neuromórfica para actuación robótica de alta velocidad (MIND-ROB). Ministerio de Ciencia, Innovación y Universidades. **IP: Linares Barranco, Alejandro**. 01/06/2020-31/05/2024. 262.812 €.
2. PCI2019-111841-2, Arquitecturas Memristivas Pulsantes para Aprender a Aprender (SMALL). Ministerio de Ciencia, Innovación y Universidades. CHISTERA-H2020. **IP: Linares Barranco**, **Alejandro**. 01/01/2020-31/07/2023. 150.000 €.
3. US-1381619, Diagnóstico asistido de señales biomédicas mediante clasificación con Deep-Learning incremental (DAFNE). Consejería de Economía, Conocimiento, Empresas y Universidad. Junta de Andalucía. **IP: Linares Barranco, Alejandro**. 01/01/2022-31/05/2023. 90.000 €.
4. TEC2016-77785-P, Sistema Cognitivo de Fusión Sensorial de Visión y Audio por Eventos (COFNET). Ministerio de Economía y Competitividad. **IP: Linares Barranco, Alejandro**. 30/12/2016-29/12/2020. 223.850 €.
5. P12-TIC-1300. Mota-Infraestructura de Sensado y Transmisión Inalámbrica para la Observación y Análisis de la Pauta de Animales Salvajes o en Semilibertad (MINERVA). Consejería de Economía, Innovación y Ciencia (Autonómico). **IP: Linares Barranco, Alejandro**. January-2014 to December-2017. 93.630 €.
6. TEC2012-37868-C04-02. Sistema Bioinspirado de Fusión Sensorial y Procesamiento Neurocortical Basado en Eventos. Aplicaciones de Alta Velocidad y Bajo Coste en Robótica y Automoción (BIOSENSE). Ministerio de Economía y Competitividad (Nacional). **IP: Linares Barranco, Alejandro.** January-2013 to December-2015. 138.645 €.
7. TEC2009-10639-C04-02. Visión ultra-rápida por eventos y sin fotogramas. Aplicación a automoción y robótica cognitiva antropomorfa (VULCANO). Ministerio de Ciencia e Innovación (Nacional). **IP: Linares Barranco, Alejandro.** January-2010 to October-2013. 104.060 € .

C.4. Contracts, technological or transfer merits
1. IPCore Sensor Neuromórfico de Audición para computación por pulso en el borde (PDC2023-145841-C33. **CoIP: Linares Barranco, Alejandro**. 01/01/24-31/12/25 74.000 €.
1. Diseño Hardware de Controladores Semafóricos para Tráfico Rodado (PCB Traffic Controller - PCBTC) Aeronaval de Construcciones e Instalaciones, S.A.. **CoIP: Linares-Barranco, Alejandro**. 15/11/2021-30/07/2022. 22.000 €.
2. AT17_5410_USE. Prototipo de dispositivo médico de apoyo al diagnóstico de cáncer de próstata mediante teorías de clasificación de imagen con Deeplearning (PROMETEO). Consejería de Economía, Conocimiento, Empresas y Universidad (Autonómico). **IP: Linares-Barranco, Alejandro.** February-2020 to December-2021. 64.725 €.
3. Neuromorphic Processor Project. Samsung Electronics Co. Ltd. **IP: Linares-Barranco, Alejandro**. 01/05/2015-30/04/2018. 273.000 €.
4. Neuromorphic Processor Project Phase 2. Samsung Electronics Co. Ltd**. IP: Linares-Barranco, Alejandro.** 01/05/2018-01/05/2020. 100.656 €.
5. Desarrollo e Implementación del Hardware y Firmware Necesario para la Automatización de un Sistema de Tinción para Inmunohistoquímica (VitroStainer). Vitro, S.A. Co-IP: Vicente Díaz, Saturnino. 14/07/2021-14/07/2023. 95.000 €.
6. Algoritmo de Planificación Genérico Adaptable a Equipos de Análisis Clínicos Automatizados (VitroPlanner). Vitro, S.A. Co-IP: Vicente Díaz, Saturnino. 14/07/2021-14/07/2023. 81.000 €
7. **Spin-off Companies**: COBER SL. http://www.t-cober.es**/ Co-founder** in 2014.