CURRICULUM VITAE ABREVIADO (CVA)

Date CVA	

Part A. PERSONAL INFORMATION

First name	Francisco Vidal		
Family name	Fernández Fernández		
Gender (*)	Male	Birth date (dd/mm/yyyy)	
Social Security, Passport, ID number			
e-mail		URL Web	
Open Researcher and Contributor ID (ORCID)		0000-0001-8682-2280	

A.1. Current position

Position	Full Professor		
Initial date	18/09/2009		
Institution	Universidad de Sevilla		
Department/Center	Instituto de Microelectrónica de Sevilla		
Country	Spain	Teleph. number	
Key words	Reliability, variability, hardware security, design methodologies, analog, mixed-signal and radiofrequency integrated circuit design		

A.2. Previous positions (research activity interuptions, indicate total months)

Period	Position/Institution/Country/Interruption cause
1/1/89 - 1/3/91	Becario F.P.I./Universidad de Sevilla/Spain
5/3/91 - 4/3/93	Ayudante de Universidad/Universidad de Sevilla/Spain
1/1/93-31/12/93	Postdoctoral fellow HCMP (Marie Curie) of European Commission/KUL/Belgium
5/3/93 - 9/2/95	Profesor Ayudante de Universidad /Universidad de Sevilla/Spain
10/2/95-17/9/09	Profesor Titular de Universidad /Universidad de Sevilla/Spain

A.3. Education

PhD, Licensed, Graduate	University/Country	Year
Licenciado en Física (Esp. Electrónica)	Universidad de Sevilla/Spain	1988
PhD in Physics. Microelectronics program	Universidad de Sevilla/Spain	1992

Part B. CV SUMMARY *(max. 5000 characters, including spaces)*

Francisco V. Fernández got his PhD degree in Physics – Microelectronics Program from the Universidad de Sevilla in 1992. In 1993 he was a postdoctoral student at Katholieke Universiteit Leuven (Belgium) funded by a HCMP fellowship (Marie Curie Program) of the European Commission. From 1995 to 2009, he was Associate Professor at the Department of Electronics and Electromagnetism of Universidad de Sevilla, where he was promoted to Full Professor in 2009. He is also with the Instituto de Microelectrónica de Sevilla (IMSE) since it was founded in 1990, and currently a joint center of CSIC and Universidad de Sevilla. He has got 5 six-year research periods awarded by ANECA and 1 technology transfer period.

He has mainly taught Electronics-related courses at the Telecommunication and Electronic Engineering degrees of the School of Engineering, at the Physics degree of the Faculty of Physics, and the Computer Engineering degree of the School of Computer Engineering, as well as several MsC and PhD programs. From 2018 to 2022, he was coordinator of the Master Program in Microelectronics: Design and Applications of Micro/Nanometric Systems of the Universidad de Sevilla. As a PhD advisor, 6 PhDs have been completed under Prof. Fernández's supervision in the past 5 years, 5 of them at the Universidad de Sevilla and 1 at Bogazici University in Turkey. Among them, Dr. F. Passos' PhD should be highlighted since it was awarded the Premio Extraordinario de Doctorado of Universidad de Sevilla in 2020 and the prestigious EDAA Outstanding Dissertation Award in 2019. It was the first and only

time in its 20 years of history that this latter award was obtained by a Spanish institution. After completing his PhD, Dr. Passos was working at a high-tech semiconductor company and currently holds a Marie Curie postdoctoral fellowship of the European Commission. All the other PhD students have successfully continued their careers after their PhD: two are working at technological companies, one is a senior researcher at IMEC, another one is working in the education sector, and another one is currently working as postdoctoral researcher at IMEC in Belgium.

Prof. Fernández's research interests lie in design and design methodologies for analog, mixed-signal and radiofrequency integrated circuits (ICs), as well as, on characterization, mitigation and exploitation of variability of (especially CMOS) ICs. Among the many contributions in these research lines some can be highlighted: development of the first symbolic circuit that became commercialized, in collaboration with two international semiconductor corporations and an EDA software vendor; the first layout-aware design methodology incorporating layout templates during the automated sizing so that accurate estimations of area and parasitics could be accounted for; the first automated multilevel (from device to sub-system) bottom-up radiofrequency circuit design methodology practically demonstrated and benchmarked in semiconductor company facilities; design of the most versatile and powerful integrated circuit for characterization of time-dependent variability, highlighted by Intel as the most important contribution in the area in 2019; the first Physical Unclonable Function (PUF) design exploiting random telegraph noise (RTN) of individual devices, with patent application in 2022; a new SRAM-based approach to true random number generation (TRNG), with patent application in 2022.

He has published about 250 research papers in international journals, books and conferences, many of them in collaboration with researchers from USA, United Kingdom, Germany, Portugal, Belgium, Mexico, China, Taiwan, Turkey, etc. According to Google Scholar his h-index is 38 (20 since 2019). He has been General Chair of three international conferences and has served at the Technical Committee Program (frequently as Programme Chair) of over 40 international conferences. From 2005 to 2015 he was Editor-in-Chief of Elsevier's Integration, the VLSI Journal and since 2003 he is Subject Editor for Analog and Mixed-Signal. He is also Founder and Chair of the Spanish Chapter of the IEEE Council on Electronic Design Automation since 2017. He has participated as researcher or principal investigator in over 25 national, international and industrial research projects, with funding of more recent and significant ones listed in section C.3. He co-founded the start-up company AnaFocus, acquired in 2014 by the global semiconductor manufacturer e2V in a 34.2M€ deal. He has participated in evaluation panels for ANEP, MICINN, MINECO, European Commission, ECSEL Joint Undertaking, AGAUR, AVAP, FWO (Belgium), IST (Portugal), UC-MEXUS (USA/Mexico). From February 2010 to December 2016 he was the TEC/MIC Collaborator of the Plan Nacional de I+D+i of Ministerio de Ciencia e Innovación and later of the Plan Estatal de I+D+i of Ministerio de Economía y Competitividad.

Part C. RELEVANT MERITS

C.1. Publications

- F. Passos, N. Lourenço, E. Roca, R. Martins, R. Castro, N. Horta and F.V. Fernández, "PACOSYT: A Passive Component Synthesis Tool Based on Machine Learning and Tailored Modeling Strategies Towards Optimal RF and mm-Wave Circuit Designs" in IEEE J. of Microwaves, vol .3, no. 2, pp. 599-613, **JCR Q1**.
- A. Santana, P. Sarazá, R. Castro, E. Roca, F.V. Fernández, Reliability improvement of SRAM PUFs based on a detailed experimental study into the stochastic effects of aging," in AEU – Int. J. of Electronics and Communications," vol 176, 2024, **JCR Q2, SJR Q2.**
- P. Sarazá, R. Castro, E. Roca, J. Martín, R. Rodríguez, M. Nafría and F.V. Fernández, "Determination of the time constant distribution of a defect-centric time-dependent variability model for sub-100-nm FETs," in IEEE Trans. on Electron Devices, vol. 69, no. 10, pp. 5424-5429, 2022. **JCR Q2, SJR Q2.**
- P. Sarazá, R. Castro, E. Roca, J. Martín, R. Rodríguez, M. Nafría and F.V. Fernández, "On the impact of the biasing history on the characterization of random telegraph noise," in IEEE Trans. on Instrumentation and Measurement, Vol. 71, 2022. **JCR Q1, SJR Q1**.
- P. Sarazá, J. Martín, R. Castro, E. Roca, R. Rodríguez, F.V. Fernández and M. Nafría, "Statistical Characterization of Time-Dependent Variability Defects Using the Maximum Current Fluctuation," in IEEE Trans. on Electron Devices, vol. 68, no. 8, pp. 4039-4044, Aug. 2021. **JCR Q2, SJR Q2.**
- J. Díaz, P. Sarazá, R. Castro, E. Roca, J. Martín, R. Rodríguez, F.V. Fernández and M. Nafría "Flexible setup for the measurement of CMOS time-dependent variability with array-based integrated circuits," IEEE Trans. on Instrumentation and Measurement, Vol. 69, No. 3, pp. 853-864, Mar. 2020. **JCR Q1, SJR Q1**.

- F. Passos, E. Roca, J. Sieiro, R. Fiorelli, R. Castro, J.M. López and F.V. Fernández, A multilevel bottom-up optimization methodology for the automated synthesis of RF systems," IEEE Trans. on Computer-Aided Design, pp. 560-571, March 2020, **JCR Q2, SJR Q2**.
- P. Sarazá-Canflanca, J. Martin-Martinez, R. Castro-Lopez, E. Roca, R. Rodriguez, M. Nafria, F.V. Fernandez, "A detailed study of the gate-drain voltage dependence of RTN in bulk pMOS transistors," Microelectronic Engineering, vol. 15, 2019. **JCR Q2, SJR Q2.**
- J. Díaz, J. Martín, R. Rodríguez, R. Castro, E. Roca, X. Aragonés, E. Barajas, D. Mateo, F.V. Fernández and M. Nafría, "A versatile CMOS transistor array IC for the statistical characterization of time-zero variability, RTN, BTI and HCI", IEEE J. of Solid-State Circuits,vol. 54, no. 2, pp 476-488, 2019. **JCR Q1, SJR Q1**.
- F. Passos, E. Roca, R. Castro and F.V. Fernández, "Radio-frequency inductor synthesis using evolutionary computation and Gaussian-process surrogate modeling," Applied Soft Computing, vol. 60, pp. 495-507, 2017. **JCR Q1, SJR Q1**.
- R. González, R. Castro, E. Roca, F.V. Fernández, J. Sieiro, J.M. López, N. Vidal, "An automated design methodology of RF circuits by using Pareto-optimal fronts of EM-simulated inductors," IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems, Vol. 36-1, pp. 15-26, 2017. **JCR Q2, SJR Q2**.

C.2. Congress

- J. Martín, J. Díaz, P. Sarazá, R. Rodríguez, R. Castro, E. Roca, F.V. Fernández and M. Nafría, "Challenges and solutions to the defect-centric modeling and circuit simulation of time-dependent variability," IEEE Int. Reliability Physics Symp., Monterey, USA, 2023. **Invited oral talk**.
- P. Sarazá, H. Carrasco, A. Santana, J. Díaz, R. Castro, E. Roca and F.V. Fernández, "A smart SRAM-cell array for the experimental study of variability phenomena in CMOS technologies," IEEE Int. Reliability Physics Symp., pp. 31-35, Dallas, USA, 2022. **Oral presentation.**
- M. Nafría, J. Díaz, P. Sarazá, J. Martín, E. Roca, R. Castro, R. Rodríguez, P. Martín, A. Toro, D. Mateo, E. Barajas. X. Aragonés and F.V. Fernández, "Circuit reliability prediction: challenges and solutions for the device time-dependent variability characterization roadblock,". IEEE Latin America Electron Devices Conf. (online), 2021. **Invited oral talk**.
- P. Sarazá, H. Carrasco, P. Brox, R. Castro, E. Roca and F.V. Fernández, "Improving the reliablity of SRAM-based PUFs under varying conditions," XXXV Conf. on Design of Circuits and Integrated Systems, Segovia, Spain, 2020. **Oral presentation. Best paper award.**
- P. Saraza-Canflanca et al., "TiDeVa: A Toolbox for the Automated and Robust Analysis of Time-Dependent Variability at Transistor Level," Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, Lausanne, Switzerland, 2019. **Oral presentation and real-time demonstration. EDA Competition winner.**
- P. Sarazá-Canflanca, J. Díaz-Fortuny, R. Castro, E. Roca, J. Martín-Martínez, R. Rodríguez, M. Nafría and F.V. Fernández, "New method for the automated massive characterization of Bias Temperature Instability in CMOS transistors," Design Automation and Test in Europe Conf., Florence, Italy, 2019. **Oral presentation.**
- F. Passos, R. Martins, N. Lourenço, E. Roca, R. Castro-López, R. Povoa, A. Canelas, N. Horta and F.V. Fernández, "Handling the effects of variability and layout parasitics in the automatic synthesis of LNAs," 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Prague, 2018. **Oral presentation. Best paper award.**
- J. Díaz-Fortuny, P. Sarazá-Canflanca, A. Toro, R. Castro, J. Martín-Martínez, E Roca, R. Rodríguez, F.V. Fernández, M. Nafría, "A Model Parameter Extraction Methodology Including Time-dependent Variability for Circuit Reliability Simulation," Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Prague, 2018. **Oral presentation. Runner-up paper award.**
- S. Ahyoune, J. Sieiro, T. Carrasco, N. Vidal, J.M. Lopez, E. Roca, F.V. Fernandez, "Extending the frequency range of quasi-static electromagnetic solvers," 14th Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Giardini Naxos, Italy, 2017. **Oral presentation. Best paper award**
- F. Passos, E. Roca, R. Castro-López and F. V. Fernández, "SIDe-O: A toolbox for surrogate inductor design and optimization," 13th Int. Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon, Portugal, 2016. **Oral presentation and real-time demonstration. EDA Competition winner.**

C.3. Research projects

Project: PID2022-136949OB-C21 / AEI / 10.13039/501100011033. Reliability, security and energy efficiency in electronic devices and circuits for IoT edge (TIRELESS-IMSE)
Principal investigators: Francisco V. Fernández and Rafael Castro López
Funding entity: Agencia Estatal de Investigación **Budget:** 203500€
Start date: 1/9/2023 **End date:** 31/8/2027 **Participation type:** Principal investigator

Project: TED2021-131240B-I00. Variabilidad temporal en circuitos integrados: enemigo y amigo (LIFELINE)
Principal investigators: Rafael Castro López and Francisco V. Fernández
Funding entity: Agencia Estatal de Investigación **Budget:** 138805€
Start date: 1/12/2022 **End date:** 30/11/2024 **Participation type:** Principal investigator

Project: PID2019-103869RB. The variability challenge in nano-CMOS: from device modeling to IC design for mitigation and exploitation (VIGILANT)
Principal investigators: Francisco V. Fernández and Rafael Castro López
Funding entity: Agencia Estatal de Investigación **Budget:** 210540€
Start date: 1/6/2020 **End date:** 31/5/2023 **Participation type:** Principal investigator

Project: TEC2016-75151-C3-3-R. Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TOGETHER)
Principal investigators: Francisco V. Fernández and Rafael Castro López
Funding entity: Ministerio de Economía y Competitividad **Budget:** 240911€
Start date: 1/1/2017 **End date:** 31/12/2019 **Participation type:** Principal investigator

Project: TEC2013-45638-C3-3-R. MARAGDA: Multilevel approach to the reliability-aware design of analog and digital integrated circuits
Principal investigator: Francisco V. Fernández
Funding entity: Ministerio de Economía y Competitividad **Budget:** 268257€
Start date: 1/1/2014 **End date:** 31/12/2018 **Participation type:** Principal investigator

Project: P12-TIC-1481. FLEXICS: Técnicas de diseño de circuitos y sistemas micro-nanoelectrónicos flexibles y reconfigurables de bajo consumo y bajo coste aplicados a comunicaciones inalámbricas
Principal investigator: Francisco V. Fernández
Funding entity: Junta de Andalucía **Budget:** 181492.5€
Start date: 1/1/2014 **End date:** 28/2/2019 **Participation type:** Principal investigator

Project: RTC-2014-2426-7. Desarrollo de kit de diseño de tecnología cerámica LTCC: modelado, simulación y fabricación de componentes y circuitos, y metodología de diseño
Principal investigator: Elisenda Roca Moreno
Call: Retos-colaboración. Programa Estatal de Investigación, Desarrollo e Innovación. 2013.
Funding entity: Ministerio de Economía y Competitividad **Budget:** 47205€
Start date: 1/9/2014 **End date:** 31/8/2016 **Participation type:** Researcher

Project: P07-TIC-02532. PLATFORM4G: Desarrollo de una plataforma de diseño de sistemas adaptables para sistemas de telecomunicaciones de cuarta generación
Principal investigator: Francisco V. Fernández
Funding entity: Junta de Andalucía **Budget:** 303000€
Start date: 31/1/2008 **End date:** 31/12/2012 **Participation type:** Principal investigator

C.4. Contracts, technological or transfer merits

Concept: Patent. **Inventors:** E. Roca, R. Castro, P. Sarazá and F.V. Fernández
Date: 24 June 2022 **Title:** Método y dispositivo para la generación de números verdaderamente aleatorios, **Patent file number** P202230569.

Concept: Patent. **Inventors:** E. Roca, R. Castro, P. Brox, E. Camacho and F.V. Fernández
Date: 18 June 2022 **Title:** Method and device for physical unclonable function (PUF) based on random telegraph noise **Patent file number** P202230344.

Concept: Start-up company **Participation type:** Co-founder **Date:** 2003-2014
Company: Innovaciones Microelectrónicas S.L. (AnaFocus). Acquired by semiconductor manufacturer e2V in 2014 with a €34.2 million deal.